IN THE SPECIFICATION:

Please replace paragraph [0007] with the following amended paragraph:

[0007] An alternative to using SEU hardened library of cells is to apply modular redundancy. Triple Modular Redundancy (TMR) is one such technique known in the art where a module is replicated three times and the output extracted from a majority voter as shown in Fig. 1, in which FIG. 1A illustrates the prior art TMR technique in block diagram form and FIG. 1B illustrates the prior art TMR technique at the gate level.

Please replace paragraph [0040] with the following amended paragraph:

With reference to ~~10 of~~ Fig. 3, an example illustrating the method employed to find the sensitivity of a gate is shown. Consider a 3-input AND gate with the signal probabilities of the inputs A, B, and C equal to 0.4, 0.6, and 0.8 respectively as shown in Fig. 2. Let the threshold probability be 0.5. The dominant value of the input gate is assigned depending upon its type. In one embodiment, if the gate is identified as an OR or NOR gate, then the dominant value of the input gate is "1" and if the gate is identified as an AND or NAND gate, then the dominant value of the input gate is "0".

Please replace paragraph [0042] with the following amended paragraph:

With reference to ~~15~~ Fig. 43, consider the 3-input gate with a different set of input probabilities. A (0.4), B (0.4) and C (0.8). The fault on line A has lesser probability of propagating through the gate as the probability of line B assuming non-dominant value is less than the threshold probability, consequently making the gate insensitive to SEUs on its inputs.

Please replace paragraph [0043] with the following amended paragraph:

With reference to Fig. 54, a method for synthesizing a hardened circuit from a given circuit is provided for a FPGA having a plurality of interconnected gates, wherein the gates have a plurality of inputs and a plurality of outputs **20**. Accordingly, the method includes identifying a plurality of primary inputs **25**, identifying a plurality of primary outputs **30**, selecting a threshold probability **35**, associating an input probability with each of the plurality of primary inputs **40**,

calculating an input probability for each of the plurality of inputs of the plurality of interconnected gates by propagating the input probability of each of the plurality of primary inputs to the corresponding plurality of primary outputs **45**, assigning a logic value to each of the plurality of inputs and the plurality of primary inputs **50**, wherein a dominant logic value is assigned to the input if the input probability is greater than the threshold probability and a non-dominant logic value is assigned to the input if the input probability is less than the threshold probability, identifying a single event upset sensitive sub-circuit by beginning at a primary output and backtracking recursively through the corresponding interconnected gates **55**. Upon identification of the single event upset sensitive sub-circuit, triple modular redundancy is then introduced for each gate of the identified single event upset sensitive sub-circuit **60**. Additionally, a voter can be introduced between each triplicated gate and the input to a nontriplicated gate **65**. The voter may be a look-up table or a tri-state buffer.

Please replace paragraph [0045] with the following amended paragraph:

In accordance with the present invention, the circuit is immunized against upsets by mitigating SEUs in the sensitive sub-circuits. This is accomplished by applying TMR for all gates in such sub-circuits. Additionally, a voter is introduced between gates depending on the fanout connections of the sensitive gates. If the fanout of a sensitive gate is connected to only sensitive gates, then the outputs of the triplicates can be directly connected to the inputs of the triplicates of the next level. This implies that the introduction of a voter between such levels is not necessary. Referring to Fig. 6A~~5~~, in an exemplary embodiment, considering the two sensitive gates identified as Gate 1 and Gate 2 (marked by dotted circles) connected as shown ~~70~~. The output D of the SEU sensitive gate, Gate 1, is connected only to Gate 2, which is also sensitive. As such, the triplicated structure for this sub-circuit is as shown in Fig. 6B~~75~~. If the fanout of the sensitive gate is connected to a non-triplicated gate, then a voter is introduced between them. The mitigated output is then fed to the non-triplicated gate. This situation is illustrated as ~~80 o~~f in Fig. 6C~~5~~, wherein the output of Gate 1, D, is connected to an SEU-sensitive gate, Gate 2, and a non-sensitive gate, Gate 3. Therefore, the outputs of the triplicated structure D_1, D_2 and D_3 have to be mitigated using a voter before it is fed to the gate of Gate 3, as shown in Fig. 6D~~85~~.

Please replace paragraph [0046] with the following amended paragraph:

In an exemplary embodiment in accordance with the present invention, consider the circuit as shown with reference to Fig. 7~~6~~. The signal probabilities of the nets are calculated as shown in Fig. 7~~8~~**0**. Gate 4 is found to be SEU sensitive as a fault on line F or line E has a high probability of affecting its output Y. Similarly, Gate 3 is sensitive as an SEU on input A, or input F, having a high probability of affecting its output X. An SEU on line Y has a high probability of affecting the signal Z2 which is the output of Gate 6, hence it is considered sensitive. Gate 5, although it has no sensitive input is considered SEU sensitive as it is in the last level of the circuit. Therefore, it is determined that Gates 3, 4, 5 and 6 are SEU sensitive as shown by the dotted circles **8~~0~~**.

Please replace paragraph [0047] with the following amended paragraph:

SEU sensitive sub-circuits are then obtained by starting at one of the outputs and backtracking through the continuous chain of sensitive gates. For example, the sub-circuit 1 can be obtained by starting at the primary output Z1. Backtracking from Gate 5, it is shown that Gate 3 and Gate 4 are sensitive gates connected to Gate 5. Backtracking recursively through Gate 3 and Gate 4, in two passes, it is shown that there are not sensitive gates when backtracking through Gate 4. Therefore, the process stops and Gate 4 and Gate 5 are marked as the sensitive gates in sub-circuit 1. Similarly, sub-circuit 2 and sub-circuit 3 as shown in the circuit of Fig. 7~~8~~**0** can be identified.

Please replace paragraph [0048] with the following amended paragraph:

TMR is now applied selectively on the subcircuits to harden the circuit against SEUs. The resulting STMR circuit is shown with reference to the circuit ~~85 of Fig. 6~~shown in Fig. 8., wherein all the gates in the sensitive sub-circuits are replaced with their triplicates. The hardened circuit has two voters introduced at the primary outputs. The voter can be implemented using either LUTs or tri-state buffers. However, it is preferred that tri-state buffers be used, as they are resistant to SEUs.

Please replace paragraph [0049] with the following amended paragraph:

It is evident from the exemplary embodiment of Fig. 7 and Fig. 8 ~~Fig. 6~~ that the SEU hardened STMR circuit has a total of 14 gates. By contrast, the same circuit when hardened by full module TRM as known in the art would result in 18 gates. As such, a savings of 4 gates is provided by the method in accordance with the present invention for the given set of input signal probabilities.

Please replace the "Brief Description of Drawings" with the following amended "Brief Description of Drawings":

For a fuller understanding of the invention, reference should be made to the following detailed description, taken in connection with the accompanying drawings, in which:

FIG. 1A and 1B is a diagrammatic view of a triple modular redundancy technique known in the prior art. FIG. 1A illustrates the prior art TMR technique in block diagram form. FIG. 1B illustrates the prior art TMR technique at the gate level.

FIG. 2 is a table illustrative of the signal probability computation at the output of a Boolean gate.

FIG. 3 is a diagrammatic view illustrating a single event upset (SEU) sensitive ~~and insensitive gates~~ gate at a $P_{threshold}$ of 0.5 in accordance with the present invention.

FIG. 4 is a diagrammatic ~~flow diagram of the method~~ view illustrating a single event upset (SEU) insensitive gate at a $P_{threshold}$ of 0.5 in accordance with the present invention.

FIG. 5 is a diagrammatic flow diagram of the method in accordance with the present invention. ~~view illustrating exemplary connections between two triplicated modules without fanout and connections between two triplicated modules with fanout.~~

FIG. 6A – 6D are ~~is~~ an diagrammatic views illustrating ~~an exemplary circuit employing the STMR method in accordance with the present invention.~~ exemplary connections between two triplicated modules without fanout and connections between two triplicated modules with fanout. FIG. 6A illustrates the connection between two sensitive gates. FIG. 6B illustrates the triplicated structure without fanout resulting from FIG. 6A in accordance with the present invention. FIG. 6C illustrates an exemplary connection between two gates. FIG. 6D illustrates the triplicated structure with fanout resulting from FIG. 6C in accordance with the present invention.

FIG. 7 is a diagrammatic view illustrating an exemplary circuit in which the SEU sensitive gates are determined and identified in accordance with the present invention.

FIG. 8 is a diagrammatic view illustrating the exemplary circuit of FIG. 7 employing the STMR method in accordance with the present invention.